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Search Results -

Terms	Documents
(silicon adj nitride) same etch same fluorocarbon$	4

US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
Database: IBM Technical Disclosure Bulletins

Search: L6

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Search History

DATE: Friday, February 15, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=DWPI; PLUR=YES; OP=ADJ			
L1	(silicon adj nitride) same etch same fluorocarbon$	14	L1
DB=USPT; PLUR=YES; OP=ADJ			
L2	(silicon adj nitride) same etch same fluorocarbon$	104	L2
DB=PGPB; PLUR=YES; OP=ADJ			
L3	(silicon adj nitride) same etch same fluorocarbon$	16	L3
DB=JPAB; PLUR=YES; OP=ADJ			
L4	(silicon adj nitride) same etch same fluorocarbon$	0	L4
DB=EPAB; PLUR=YES; OP=ADJ			
L5	(silicon adj nitride) same etch same fluorocarbon$	3	L5
DB=TDBD; PLUR=YES; OP=ADJ			
L6	(silicon adj nitride) same etch same fluorocarbon$	4	L6

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 14 of 14 returned.

1. Document ID: JP 2001176842 A, US 2001005636 A1

L1: Entry 1 of 14 File: DWPI Jun 29, 2001

DERWENT-ACC-NO: 2001-475234
DERWENT-WEEK: 200152

TITLE: Etching of silicon nitride film in semiconductor fabrication using mixture of fluorocarbon gas and inert gas

Standard Title Terms:
ETCH SILICON NITRIDE FILM SEMICONDUCTOR FABRICATE MIXTURE FLUOROCARBON GAS INERT GAS

Standard Title Terms (1):
ETCH SILICON NITRIDE FILM SEMICONDUCTOR FABRICATE MIXTURE FLUOROCARBON GAS INERT GAS

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Drawu Desc | Image

2. Document ID: JP 2000286241 A

L1: Entry 2 of 14 File: DWPI Oct 13, 2000

DERWENT-ACC-NO: 2001-084254
DERWENT-WEEK: 200110

TITLE: Semiconductor device manufacturing method involves injecting specific fluorocarbon gas mixed with specific addition gas onto silicon nitride film, during dry etching

Standard Title Terms:
SEMICONDUCTOR DEVICE MANUFACTURE METHOD INJECTION SPECIFIC FLUOROCARBON GAS MIX SPECIFIC ADD GAS SILICON NITRIDE FILM DRY ETCH

Standard Title Terms (1):
SEMICONDUCTOR DEVICE MANUFACTURE METHOD INJECTION SPECIFIC FLUOROCARBON GAS MIX SPECIFIC ADD GAS SILICON NITRIDE FILM DRY ETCH

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Drawu Desc | Image

3. Document ID: US 6069087 A

L1: Entry 3 of 14 File: DWPI May 30, 2000

DERWENT-ACC-NO: 2000-410875
DERWENT-WEEK: 200035

TITLE: One-step plasma etching process for selectively etching silicon dielectrics, e.g., silicon nitride, involves exposing the layer to be etched to a plasma formed from a mixture of fluorocarbon gases

Standard Title Terms:
ONE STEP PLASMA ETCH PROCESS SELECT ETCH SILICON DIELECTRIC SILICON NITRIDE EXPOSE LAYER ETCH PLASMA FORMING MIXTURE FLUOROCARBON GAS

Standard Title Terms (1):
ONE STEP PLASMA ETCH PROCESS SELECT ETCH SILICON DIELECTRIC SILICON NITRIDE EXPOSE LAYER ETCH PLASMA FORMING MIXTURE FLUOROCARBON GAS

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4. Document ID: US 5994229 A

L1: Entry 4 of 14 File: DWPI Nov 30, 1999

DERWENT-ACC-NO: 2000-085340
DERWENT-WEEK: 200007

TITLE: Shallow trench forming method used in integrated circuit manufacture

Basic Abstract Text:
DETAILED DESCRIPTION - A pad oxide film (3), silicon nitride film (4) and photoresist film (5) are formed sequentially on Si substrate (2). Then, photoresist layer is patterned to define the trench's length and width. The silicon nitride film is removed by reactive ion etching by applying pressure of 30-150 millitorr, simultaneously admitting methane trifluoride, carbon tetrafluoride, argon and oxygen at flow rate between 5-30, 5-45, 50-200, 100 SCCM respectively and initiating glow discharge at power level of about 300-900 watts. Using optical emission spectroscopy, the reactive ion etching is terminated. The pad oxide film is etched by another reactive ion etching by applying pressure of 50-150 millitorr, simultaneously admitting gas selected from group containing methane trifluoride, polymer forming fluorocarbon and fluorinated hydrocarbon, methane monofluoride and argon at flow rate between 5-20, 5-20 and 5-150 SCCM respectively and initiating glow discharge at power level between 500-1200 watts. After elapse of predetermined time, the etching of pad oxide film is terminated. Then, breakthrough etch is performed at a pressure of 50-150 millitorr, simultaneously admitting carbon tetrafluoride at about 15-50 SCCM and initiating glow discharge at power level of about 300-600 watts. Then, breakthrough etching is terminated after elapse of 5-30 seconds. After terminating selective silicon etching to silicon substrate at predetermined time elapse, photoresist layer is removed.

Basic Abstract Text (2):
DETAILED DESCRIPTION - A pad oxide film (3), silicon nitride film (4) and photoresist film (5) are formed sequentially on Si substrate (2). Then, photoresist layer is patterned to define the trench's length and width. The silicon nitride film is removed by reactive ion etching by applying pressure of 30-150 millitorr, simultaneously admitting methane trifluoride, carbon tetrafluoride, argon and oxygen at flow rate between 5-30, 5-45, 50-200, 100 SCCM respectively and initiating glow discharge at power level of about 300-900 watts. Using optical emission spectroscopy, the reactive ion etching is terminated. The pad oxide film is etched by another reactive ion etching by applying pressure of 50-150 millitorr, simultaneously admitting gas selected from

group containing methane trifluoride, polymer forming fluorocarbon and fluorinated hydrocarbon, methane monofluoride and argon at flow rate between 5-20, 5-20 and 5-150 SCCM respectively and initiating glow discharge at power level between 500-1200 watts. After elapse of predetermined time, the etching of pad oxide film is terminated. Then, breakthrough etch is performed at a pressure of 50-150 millitorr, simultaneously admitting carbon tetrafluoride at about 15-50 SCCM and initiating glow discharge at power level of about 300-600 watts. Then, breakthrough etching is terminated after elapse of 5-30 seconds. After terminating selective silicon etching to silicon substrate at predetermined time elapse, photoresist layer is removed.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

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5. Document ID: JP 11186224 A

L1: Entry 5 of 14 File: DWPI Jul 9, 1999

DERWENT-ACC-NO: 1999-450060
DERWENT-WEEK: 200029

TITLE: Self-aligned contact hole formation of bit-line contact in DRAM - by etching silicon nitride film and portion of silicon oxide film which is not etched, using fluorocarbon group and carbon mon:oxide gas with hydrogen bond

Standard Title Terms:
SELF ALIGN CONTACT HOLE FORMATION BIT LINE CONTACT DRAM ETCH SILICON NITRIDE FILM PORTION SILICON OXIDE FILM ETCH FLUOROCARBON GROUP CARBON MONO OXIDE GAS HYDROGEN BOND
Standard Title Terms (1):
SELF ALIGN CONTACT HOLE FORMATION BIT LINE CONTACT DRAM ETCH SILICON NITRIDE FILM PORTION SILICON OXIDE FILM ETCH FLUOROCARBON GROUP CARBON MONO OXIDE GAS HYDROGEN BOND

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

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6. Document ID: US 5843846 A

L1: Entry 6 of 14 File: DWPI Dec 1, 1998

DERWENT-ACC-NO: 1999-044614
DERWENT-WEEK: 199904

TITLE: Rounding top corners of submicron silicon trenches - by etching with fluorocarbon argon nitrogen gas combination

Ba sic Abstract Text:
A method of rounding the top corners (265) of a trench in a semiconductor device comprises etching to round the corners using a fluorocarbon/argon/n itrogen gas mixture while maintaining critical dimension control. Also claimed is a method as above in which a silicon nitride layer is deposited and laterally etched to expose and round the top corners as the trench is formed. Preferably, the fluorocarbon is CF4, the substrate is silicon and etching is performed in a low density parallel plate etch reactor.
Basic Abstract Text (1):
A method of rounding the top corners (265) of a trench in a semiconductor device comprises etching to round the corners using a fluorocarbon/argon/n itrogen gas mixture while maintaining critical dimension control. Also claimed is a method as above in

which a silicon nitride layer is deposited and laterally etched to expose and round the top corners as the trench is formed. Preferably, the fluorocarbon is CF4, the substrate is silicon and etching is performed in a low density parallel plate etch reactor.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 7. Document ID: JP 09129608 A

L1: Entry 7 of 14 File: DWPI May 16, 1997

DERWENT-ACC-NO: 1997-325937
DERWENT-WEEK: 199730
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TITLE: Etching silicon nitride and silicon oxide film - involves applying neutral fluorocarbon particles to surface before exposure to argon ions

Standard Title Terms:
ETCH SILICON NITRIDE SILICON OXIDE FILM APPLY NEUTRAL FLUOROCARBON PARTICLE SURFACE EXPOSE ARGON ION< br>
Standard Title Terms (1):
ETCH SILICON NITRIDE SILICON OXIDE FILM APPLY NEUTRAL FLUOROCARBON PARTICLE SURFACE EXPOSE ARGON ION

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 8. Document ID: JP 08111405 A

L1: Entry 8 of 14 File: DWPI Apr 30, 1996

DERWENT-ACC-NO: 1996-265776
DERWENT-WEEK: 199627
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TITLE: Semiconductor device mfg method - involves forming silicon oxide, poly- and nitride films, resist, silicon nitride mask, then etching with fluorocarbon gas

Standard Title Terms:
SEMICONDUCTOR DEVICE MANUFACTURE METHOD FORMING SILICON OXIDE POLY NITRIDE FILM RESIST SILICON NITRIDE MASK ETCH FLUOROCARBON GAS

Standard Title Terms (1):
SEMICONDUCTOR DEVICE MANUFACTURE METHOD FORMING SILICON OXIDE POLY NITRIDE FILM RESIST SILICON NITRIDE MASK ETCH FLUOROCARBON GAS

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 9. Document ID: US 5503901 A, JP 07074145 A

L1: Entry 9 of 14 File: DWPI Apr 2, 1996

DERWENT-ACC-NO: 1995-150389
DERWENT-WEEK: 199619

TITLE: Surface processing method for semiconductor device mfr. using fluorocarbon gas - selectively etching silicon oxide film to silicon nitride film while generating CF2 ions

Standard Title Terms:
SURFACE PROCESS METHOD SEMICONDUCTOR DEVICE MANUFACTURE FLUOROCARBON GAS SELECT ETCH SILICON OXIDE FILM SILICON NITRIDE FILM GENERATE ION

Standard Title Terms (1):
SURFACE PROCESS METHOD SEMICONDUCTOR DEVICE MANUFACTURE FLUOROCARBON GAS SELECT ETCH SILICON OXIDE FILM SILICON NITRIDE FILM GENERATE ION

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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10. Document ID: KR 274080 B, US 5366590 A, JP 06275568 A

L1: Entry 10 of 14 File: DWPI Dec 15, 2000

DERWENT-ACC-NO: 1995-005718
DERWENT-WEEK: 200174

TITLE: Dry etching method - using fluorocarbon gas for high selectivity etching of silicon di:oxide on silicon nitride

Stand ard Title Terms:
DRY ETCH METHOD FLUOROCARBON GAS HIGH SELECT ETCH SILICON DI OXIDE SILICON NITRIDE

Standard Title Terms (1):
DRY ETCH METHOD FLUOROCARBON GAS HIGH SELECT ETCH SILICON DI OXIDE SILICON NITRIDE

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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11. Document ID: US 5286344 A

L1: Entry 11 of 14 File: DWPI Feb 15, 1994

DERWENT-ACC-NO: 1994-057137
DERWENT-WEEK: 199917

TITLE: Multilayer structure plasma etching process to form etched pattern esp. with selective silicon di:oxide etching on silicon nitride layer - using fluorinated chemical etchant system with fluorocarbon additive material having number of hydrogen atoms equal to or greater than number of fluorine atoms and reactive gas etchant or ion etchant

Standard Title Terms:
MULTILAYER STRUCTURE PLASMA ETCH PROCESS FORM ETCH PATTERN SELECT SILICON DI OXIDE ETCH SILICON NITRIDE LAYER FLUORINATED CHEMICAL ETCH SYSTEM FLUOROCARBON ADDITIVE MATERIAL NUMBER HYDROGEN ATOM EQUAL GREATER NUMBER FLUORINE ATOM REACT GAS ETCH ION ETCH

Standard Title Terms (1):
MULTILAYER STRUCTURE PLASMA ETCH PROCESS FORM ETCH PATTERN SELECT SILICON DI OXIDE ETCH SILICON NITRIDE LAYER FLUORINATED CHEMICAL ETCH SYSTEM FLUOROCARBON ADDITIVE MATERIAL NUMBER HYDROGEN ATOM EQUAL GREATER NUMBER FLUORINE ATOM REACT GAS ETCH ION ETCH

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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12. Document ID: DE 3420347 A, DE 3420347 C, JP 59222933 A, JP 60115232 A, NL 8401774 A, US 4529476 A

L1: Entry 12 of 14 File: DWPI Dec 6, 1984

DERWENT-ACC-NO: 1984-308078
DERWENT-WEEK: 198450

TITLE: Selective gas etching of silicon nitride - using gas contg. fluorohydrocar bon

Standard Title Terms:
SELECT GAS ETCH SILICON NITRIDE GAS CONTAIN FLUOROCARBON

Standard Title Terms (1):
SELECT GAS ETCH SILICON NITRIDE GAS CONTAIN FLUOROCARBON

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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13. Document ID: JP 56091447 A

L1: Entry 13 of 14 File: DWPI Jul 24, 1981

DERWENT-ACC-NO: 1981-66636D
DERWENT-WEEK: 198137

TITLE: Element isolation regions formation in semiconductor devices - using an etching process involving use of fluorocarbon gas for etching of silicon nitride mask

Standard Title Terms:
ELEMENT ISOLATE REGION FORMATION SEMICONDUCTOR DEVICE ETCH PROCESS FLUOROCARBON GAS ETCH SILICON NITRIDE MASK

Standard Title Terms (1):
ELEMENT ISOLATE REGION FORMATION SEMICONDUCTOR DEVICE ETCH PROCESS FLUOROCARBON GAS ETCH SILICON NITRIDE MASK

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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14. Document ID: JP 56091446 A

L1: Entry 14 of 14 File: DWPI Jul 24, 1981

DERWENT-ACC-NO: 1981-66635D
DERWENT-WEEK: 198137

TITLE: Silica element isolation regions formation - using an etching process involving use of fluorocarbon for etching of silicon nitride mask

Standard Title Terms:
SILICA ELEMENT ISOLATE REGION FORMATION ETCH PROCESS FLUOROCARBON ETCH SILICON NITRIDE MASK

Standard Title Terms (1):
SILICA ELEMENT ISOLATE REGION FORMATION ETCH PROCESS FLUOROCARBON ETCH SILICON NITRIDE MASK

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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Terms	Documents
(silicon adj nitride) same etch same fluorocarbon$	14

Display Format: KWIC Change Format

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Search Results - Record(s) 1 through 16 of 16 returned.

1. Document ID: US 20020012876 A1

L3: Entry 1 of 16 File: PGPB Jan 31, 2002

PGPUB-DOCUMENT-NUMBER: 20020012876
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020012876 A1

TITLE: Tunable vapor deposited materials as antireflective coatings, hardmasks and as combined antireflective coating/hardmasks and methods of fabrication thereof and applications thereof

PUBLICATION-DATE: January 31, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Angelopoulos, Marie	Cortlandt	NY	US	
Babich, Katherina	Chappaqua	NY	US	
Grill, Alfred	White Plains	NY	US	
Halle, Scott David	Hopewell Junction	NY	US	
Mahorowala, Arpan Pravin	White Plains	NY	US	
Patel, Vishnubhai Vitthalbhai	Yorktown Heights	NY	US	

US-CL-CURRENT: 430/271.1; 430/314, 430/315, 430/325, 430/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

2. Document ID: US 20020011673 A1

L3: Entry 2 of 16 File: PGPB Jan 31, 2002

PGPUB-DOCUMENT-NUMBER: 20020011673
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020011673 A1

TITLE: Process and structure for an interlock and high performance multilevel structures for chip interconnects and packaging technologies

PUBLICATION-DATE: January 31, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Uzoh, Cyprian E.	Milpitas	CA	US	

US-CL-CURRENT: 257/758; 257/774

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 3. Document ID: US 20020001952 A1

L3: Entry 3 of 16 File: PGPB Jan 3, 2002

PGPUB-DOCUMENT-NUMBER: 20020001952
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020001952 A1

TITLE: Non metallic barrier formations for copper damascene type interconnects

PUBLICATION-DATE: January 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Chooi, Simon	Singapore		SG	
Gupta, Subhash	Singapore		SG	
Zhou, Mei-Sheng	Singapore		SG	
Hong, Sangki	Singapore		SG	

US-CL-CURRENT: 438/687

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 4. Document ID: US 20020001951 A1

L3: Entry 4 of 16 File: PGPB Jan 3, 2002

PGPUB-DOCUMENT-NUMBER: 20020001951
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020001951 A1

TITLE: Non metallic barrier formations for copper damascene type interconnects

PUBLICATION-DATE: January 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Chooi, Simon	Singapore		SG	
Gupta, Subhash	Singapore		SG	
Zhou, Mei-Sheng	Singapore		SG	
Hong, Sangki	Singapore		SG	

US-CL-CURRENT: 438/687

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 5. Document ID: US 20020000423 A1

L3: Entry 5 of 16 File: PGPB Jan 3, 2002

PGPUB-DOCUMENT-NUMBER: 20020000423
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020000423 A1

TITLE: Method for enhancing oxide to nitride selectivity through the use of independent heat control

PUBLICATION-DATE: January 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Becker, David S.	Boise	ID	US	
Blalock, Guy T.	Boise	ID	US	
Roe, Fred L.	San Jose	CA	US	

US-CL-CURRENT: 216/67; 216/2, 216/79

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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6. Document ID: US 20010055878 A1

L3: Entry 6 of 16 File: PGPB Dec 27, 2001

PGPUB-DOCUMENT-NUMBER: 20010055878
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010055878 A1

TITLE: Non-conductive barrier formations for copper damascene type interconnects

PUBLICATION-DATE: December 27, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Chooi, Simon	Singapore		SG	
Gupta, Subhash	Singapore		SG	
Zhou, Mei-Sheng	Singapore		SG	
Hong, Sangki	Singapore		SG	

US-CL-CURRENT: 438/687

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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7. Document ID: US 20010049195 A1

L3: Entry 7 of 16 File: PGPB Dec 6, 2001

PGPUB-DOCUMENT-NUMBER: 20010049195
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010049195 A1

TITLE: Non-metallic barrier formations for copper damascene type interconnects

PUBLICATION-DATE: December 6, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Chooi, Simon	Singapore		SG	
Gupta, Subhash	Singapore		SG	
Zhou, Mei-Sheng	Singapore		SG	
Hong, Sangki	Singapore		SG	

US-CL-CURRENT: 438/687

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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8. Document ID: US 20010038972 A1

L3: Entry 8 of 16 File: PGPB Nov 8, 2001

PGPUB-DOCUMENT-NUMBER: 20010038972
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010038972 A1

TITLE: ULTRA-THIN RESIST SHALLOW TRENCH PROCESS USING METAL HARD MASK

PUBLICATION-DATE: November 8, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
LYONS, CHRISTOPHER F.	FREMONT	CA	US	
BELL, SCOTT A.	SAN JOSE	CA	US	
LEVINSON, HARRY J.	SARATOGA	CA	US	
NGUYEN, KHANH B.	SAN MATEO	CA	US	
WANG, FEI	SAN JOSE	CA	US	
YANG, CHIH YUH	SAN JOSE	CA	US	

US-CL-CURRENT: 430/313; 430/311, 430/316, 430/423, 430/424, 430/432

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

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9. Document ID: US 20010021576 A1

L3: Entry 9 of 16 File: PGPB Sep 13, 2001

PGPUB-DOCUMENT-NUMBER: 20010021576
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010021576 A1

TITLE: Method of manufacturing self-aligned contact hole

PUBLICATION-DATE: September 13, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Chi, Kyeong-koo	Seoul		KR	
Nam, Byeong-yun	Suwon-city		KR	

US-CL-CURRENT: 438/586; 438/592

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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10. Document ID: US 20010012694 A1

L3: Entry 10 of 16 File: PGPB Aug 9, 2001

PGPUB-DOCUMENT-NUMBER: 20010012694
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010012694 A1

TITLE: Plasma etching method using low ionization potential gas

PUBLICATION-DATE: August 9, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Coburn, John W.	San Jose	CA	US	
Donohoe, Kevin G.	Boise	ID	US	

US-CL-CURRENT: 438/689

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

11. Document ID: US 20010012653 A1

L3: Entry 11 of 16 File: PGPB Aug 9, 2001

PGPUB-DOCUMENT-NUMBER: 20010012653
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010012653 A1

TITLE: METHOD FOR FABRICATING MOS TRANSISTORS

PUBLICATION-DATE: August 9, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
TSUKAMOTO, MASANORI	KANAGAWA		JP	

US-CL-CURRENT: 438/197

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

12. Document ID: US 20010009291 A1

L3: Entry 12 of 16 File: PGPB Jul 26, 2001

PGPUB-DOCUMENT-NUMBER: 20010009291
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010009291 A1

TITLE: Semiconductor structure having reduced silicide resistance between closely spaced gates and method of fabrication

PUBLICATION-DATE: July 26, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Miles, Glen L.	Essex Junction	VT	US	

US-CL-CURRENT: 257/382; 257/288, 257/368, 257/369, 257/377, 257/383, 257/384, 257/900, 438/184, 438/197, 438/199, 438/230, 438/265, 438/300, 438/303, 438/595

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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13. Document ID: US 20010008226 A1

L3: Entry 13 of 16 File: PGPB Jul 19, 2001

PGPUB-DOCUMENT-NUMBER: 20010008226
PGPUB-FILING-TYPE: new-utility
DOCUMENT-IDENTIFIER: US 20010008226 A1

TITLE: IN-SITU INTEGRATED OXIDE ETCH PROCESS PARTICULARLY USEFUL FOR COPPER DUAL DAMASCENE

PUBLICATION-DATE: July 19, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
HUNG, HOIMAN	SAN JOSE	CA	US	
CAULFIELD, JOSEPH P.	LAFAYETTE	CA	US	
TANG, SUM-YEE BETTY	SAN JOSE	CA	US	
DING, JIAN	SAN JOSE	CA	US	
XU, TIANZONG	MOUNTAIN VIEW	CA	US	

US-CL-CURRENT: 216/18; 216/39, 216/67, 216/68, 216/72, 216/80, 252/79.1, 438/695

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

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14. Document ID: US 20010005636 A1

L3: Entry 14 of 16 File: PGPB Jun 28, 2001

PGPUB-DOCUMENT-NUMBER: 20010005636
PGPUB-FILING-TYPE: new-utility
DOCUMENT-IDENTIFIER: US 20010005636 A1

TITLE: Method of etching silicon nitride film and method of producing semiconductor device

PUBLICATION-DATE: June 28, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Nishizawa, Atsushi	Tokyo		JP	

US-CL-CURRENT: 438/710; 438/689, 438/712

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

15. Document ID: US 20010004552 A1

L3: Entry 15 of 16 File: PGPB Jun 21, 2001

PGPUB-DOCUMENT-NUMBER: 20010004552
PGPUB-FILING-TYPE: new-utility
DOCUMENT-IDENTIFIER: US 20010004552 A1

TITLE: Plasma etch process in a single inter-level dielectric etch

PUBLICATION-DATE: June 21, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Tang, Betty	San Jose	CA	US	
Ding, Jian	San Jose	CA	US	

US-CL-CURRENT: 438/689; 438/710, 438/712

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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16. Document ID: US 20010000246 A1

L3: Entry 16 of 16 File: PGPB Apr 12, 2001

PGPUB-DOCUMENT-NUMBER: 20010000246
PGPUB-FILING-TYPE: new-utility
DOCUMENT-IDENTIFIER: US 20010000246 A1

TITLE: Plasma etch process in a single inter-level dielectric etch

PUBLICATION-DATE: April 12, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Tang, Betty	San Jose	CA	US	
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US-CL-CURRENT: 438/689; 438/710, 438/712

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

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Terms	Documents
(silicon adj nitride) same etch same fluorocarbon$	16

Display Format: CIT Change Format

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Search Results - Record(s) 1 through 3 of 3 returned.

1. Document ID: US 5817579 A

L5: Entry 1 of 3 File: EPAB Oct 6, 1998

DOCUMENT-IDENTIFIER: US 5817579 A
TITLE: Two step plasma etch method for forming self aligned contact

Abstract (1):
CHG DATE=19990617 STATUS=N>A method for forming a via through a silicon oxide layer. There is first provided a substrate. There is then formed over the substrate a patterned silicon nitride layer which defines a contact beneath the patterned silicon nitride layer. There is then formed over the patterned silicon nitride layer a silicon oxide layer. There is then etched the silicon oxide layer through a first reactive ion etch (RIE) method employing a first etchant gas composition comprising a fluorocarbon etchant gas to form: (1) an etched silicon oxide layer which exposes the contact without substantially etching the patterned silicon nitride layer; and (2) a fluorocarbon polymer residue layer formed upon at least one of the etched silicon oxide layer and the patterned silicon nitride layer. Finally, there is stripped from the substrate the fluorocarbon polymer residue layer through a second reactive ion etch (RIE) method employing a second etchant gas composition comprising carbon tetrafluoride and oxygen. The method may also be employed in general for etching silicon oxide layers in the presence of silicon nitride layers. Similarly, the method may also in general be employed in removing fluorocarbon polymer residue layers from integrated circuit layers including but not limited to silicon oxide layers and silicon nitride layers.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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2. Document ID: US 5286344 A

L5: Entry 2 of 3 File: EPAB Feb 15, 1994

DOCUMENT-IDENTIFIER: US 5286344 A
TITLE: Process for selectively etching a layer of silicon dioxide on an underlying stop layer of silicon nitride

Abstract (1):
More specifically, a process is provided for etching a multilayer structure to form a predetermined etched pattern therein. The subject process comprises providing the multilayer structure having a plurality of structural layers. The structural layers of the multilayer structure comprise a silicon dioxide outer layer on an underlying silicon nitride stop layer. Then, a chemical etchant protective layer is formed on a major surface of the multilayer structure having a predetermined pattern of openings, thereby exposing areas of the silicon dioxide outer layer corresponding to the predetermined pattern of openings. The exposed areas of the silicon dioxide outer layer are then etched down to the silicon nitride stop layer, at a high SiO_2 etch rate and at a high level of selectivity of the SiO_2 etch rate with respect to the Si_3N_4 etch rate, with a fluorinated chemical etchant system. The fluorinated chemical etchant system

includes an etchant material and an additive material. The additive material comprises a fluorocarbon material in which the number of hydrogen atoms is equal to or greater than the number of fluorine atoms. The etching step forms a substantially predetermined etch pattern in the silicon dioxide outer layer in which the contact sidewalls of said SiO2 outer layer are substantially upright.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 3. Document ID: EP 265584 A2

L5: Entry 3 of 3 File: EPAB May 4, 1988

DOCUMENT-IDENTIFIER: EP 265584 A2
TITLE: Method and materials for etching silicon dioxide using silicon nitride or silicon rich dioxide as an etch barrier.

Abstract (1):
A process for etching SiO2 using either silicon rich SiO2 or Si2N4 as an etching barrier over a substrate. Selectivity is obtained between the two dielectric materials, silicon dioxide and silicon nitride or silicon dioxide and silicon rich silicon dioxide wherein the oxide etches considerably faster than nitride (or silicon rich silicon dioxide) because of the selectivity of oxide to nitride. A further object of the present invention is to provide an etching process wherein the silicon dioxide on the substrate is directionally etched in a fluorocarbon gas to form silicon dioxide spacers on a substrate, and the substrate surface ist protected by an etch stop composed of the silicon nitride or silicon rich silicon dioxide material.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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Terms	Documents
(silicon adj nitride) same etch same fluorocarbon$	3

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Search Results - Record(s) 1 through 4 of 4 returned.

☐ 1. Document ID: NN87013724

L6: Entry 1 of 4 File: TDBD Jan 1, 1987

TDB-ACC-NO: NN87013724

DISCLOSURE TITLE: Multiple Sidewall Process for Trench Masks

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, January 1987, US

VOLUME NUMBER: 29
ISSUE NUMBER: 8
PAGE NUMBER: 3724 - 3725

PUBLICATION-DATE: January 1, 1987 (19870101)

CROSS REFERENCE: 0018-8689-29-8-3724

DISCLOSURE TEXT:

- This article relates generally to integrated circuit fabrication and, more particularly, to the formation of trenches having high aspect ratios. Deep, narrow trenches of sub-micron dimensions can be formed with standard optical lithography by first etching a wide trench and reconstructing walls to form narrow trenches. In Fig. 1, oxide layer 1 is either deposited or grown on substrate 2 to the thickness necessary to mask the trench etching. Layer 1 is masked and an area is etched with a fluorocarbon and hydrogen to leave wide trench 3 with a shallow oxide coating 4 at the bottom of the trench. In Fig. 2, silicon nitride spacers 5 are formed on the trench sidewalls, followed by deposition of silicon dioxide spacers 6 on spacers 5. The oxide surface is again oxidized for protection. In the next step seen in Fig. 3, nitride spacers are removed by a highly selective wet chemical or dry etch, such as hot phosphoric acid or a fluorocarbon and oxygen plasma etch. This leaves trenches 7 that can be transferred into the silicon. This process permits the nitride deposition to determine the trench widths and their spacing to be controlled by the oxide deposition. The number of trenches is controlled by the original area imaged.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Clip Img

☐ 2. Document ID: NN86102184

L6: Entry 2 of 4 File: TDBD Oct 1, 1986

TDB-ACC-NO: NN86102184

DISCLOSURE TITLE: Punch-Through Guard Ring for Butted Transistor Emitters

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, October 1986, US

VOLUME NUMBER: 29
ISSUE NUMBER: 5
PAGE NUMBER: 2184 - 2185

PUBLICATION-DATE: October 1, 1986 (19861001)

CROSS REFERENCE: 0018-8689-29-5-2184

DISCLOSURE TEXT:

- This article relates generally to semiconductor fabrication and, more particularly, to construction of guard rings for butted emitters to prevent punch-through. A single added implantation step during fabrication of NPN transistors having butted emitters produces a thicker guard ring to prevent emitter-collector punch-through. The construction process is as follows: In Fig. 1, layers of silicon dioxide 1 and silicon nitride 2 are deposited on silicon substrate 3. Photoresist 4 is deposited, exposed and developed to define the active device region. Boron implantation is performed through layers 1 and 2 and produces "transverse straggle" in areas 5 to form the guard ring beneath layer 1 and the mask opening. In Fig. 2, reactive ion etching (RIE) is then used to form an opening through the exposed silicon dioxide 1 and silicon nitride 2 into substrate 3. RIE is important since it does not etch laterally to remove implanted boron beneath photoresist 4. Thereafter, the photoresist is stripped and recessed oxide is grown. During this latter step, the boron ions in implantation areas 5 diffuse outwardly enlarging those areas at the edges of the recessed oxide 6, forming the guard ring. Silicon dioxide layer 1 and silicon nitride layer 2 are then removed, as in Fig. 3, and p-type intrinsic base 7 and n-polysilicon emitter 8 are formed. Arsenic ions from the emitter diffuse into the silicon to form a shallow n emitter region 9. It will be noted that the p-type intrinsic base is thinned at the butted edges due to processing steps. The thicker guard ring causes no performance degradation and the doping level of the guard ring can be controlled by varying the boron implantation dose. A variation in the guard ring formation is to strip the photoresist after boron implantation, then perform high temperature annealing. This drives the boron further beneath the nitride stack. Reactive ion etching is done in a fluorocarbon-oxygen atmosphere to minimize nitride removal.

☐ 3. Document ID: NB83046131

L6: Entry 3 of 4 File: TDBD Apr 1, 1983

TDB-ACC-NO: NB83046131

DISCLOSURE TITLE: Processes to Reduce and Control the P Type Doping Concentration at the Boundary Between Recessed Oxide and Active Device Regions. April 1983.

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, April 1983, US

VOLUME NUMBER: 25
ISSUE NUMBER: 11B
PAGE NUMBER: 6131 - 6142

PUBLICATION-DATE: April 1, 1983 (19830401)

CROSS REFERENCE: 0018-8689-25-11B-6131

DISCLOSURE TEXT:

12p. In the conventional fabrication of recessed thick silicon dioxide, commonly used to isolate MOSFETs and N/+/ diffusions, the boron concentration thereunder is increased by means of ion implantation of boron. There results high threshold voltage for the recessed silicon dioxide without having to grow it extremely thick. After the implantation, several heat cycles grow thick and thin silicon dioxide. Consequently, the implanted boron under the thick silicon dioxide spreads into non recessed silicon dioxide regions wherein MOSFET's and N diffusions are formed. This situation is illustrated by the cross-section of Fig. 1 along the width direction of a MOSFET and an N/+/ diffusion. - In Fig. 1, it is noticed that the P-type doping concentration surrounding the perimeter of the N/+/ diffusion has been increased by the spread of the boron implanted under the recessed silicon dioxide isolation (ROI). This leads to increased perimeter junction capacitance (Cp), by a factor of 2 or 3 and lowered junction breakdown voltage, threshold voltage then goes up with narrowing channel width as the extent of the boron penetration becomes comparable with it. Over a distribution of MOSFET devices, this effect increases the threshold voltage sigma since boron spread does not track channel width. This effect is distinct from the well-known rise in threshold voltage when the total depleted bulk charge adjacent to the channel edges is large relative to the bulk charge under the channel. This second width efffect on threshold voltage is probably intensified by increased boron doping around the channel edges since the adjacent depleted bulk charge is proportional to the (boron doping)(see original).K In addition to these adverse electrical effects, conventional growth of recessed silicon dioxide also produces the "bird's beak" structure which sets the minimum width of the isolating field regions in a VLSI chip at a higher level than required by electrical or photo graphic considerations. Such minimum width can be reduced by growing less thick silicon dioxide. However, if the thick silicon doxide threshold voltage, is to remain unchanged, the circuits have to be designed to absorb higher Cp, lower BV, and higher active device threshold voltage all resulting from having to increase boron dosage to compensate for the less thick field silicon dioxide. - In what follows, four fabrication sequences are described to offset the field boron implant away from the perimeter of the active device regions so that the boron concentration at the common boundary of field and active regions can be independently set at a level different from that inside the field regions. The first process sequence yields a semi-recessed field oxide structure, while the others yield fully recessed field oxide structures. Measures are taken in all processes to prevent the growth of bird's beak. - The first process sequence to offset the field implant and avoid bird'; beak is as follows: (1) Start with a P-type substrate 1. Thermally grow a 50 nm silicon dioxide layer 2. Next, use chemical vapor deposition (CVD), to form a silicon nitride layer 4 of 50 nm in thickness. Polysilicon layer 6 is then deposited to about 250 nm. Its conductivity is made N/+/ by phosphorus doping from a POCl source, and thus enhances the oxidation rate during step (4) below. A second silicon nitride layer 8 is deposited on 6 to be twice as thick as the first silicon nitride layer 4, as seen in Fig. 2. - (2) Spin a positive photoresist layer on layer 8 and define field regions 9 using a first masking operation. Harden the developed photo resist in a fluorocarbon plasma. - (3) Reactive ion etch (RIE) through layers 8 and 6 to expose layer 4. - Active device regions 10 are ~eft covered with pedestals composed of polysilicon layers 6 and silicon nitride layer 8. Having used RIE, the pedestal sidewalls 6' are almost vertical. At this point, a low dose boron implant may he used to form a P-type subsurface layer 12 of higher concentration than that of the substrate 1, as shown by Fig. 3. The P-type concentration of layer 12 should be chosen just high enough to avoid inversion problems around the perimeter of active device regions 10. - (4) Cover polysilicon sidewalls 6' with a thermal silicon dioxide wall 14 of a thickness designed to offset the perimeter of the subsequent boron field implant away from the device regions 10. For state of the art processing, a 500 nm thick wall is adequate and requires about one hour of wet oxidation of the N/+/ polysilicon layer 6. - Notice that the perimeter of the active device regions 10, as defined by the sidewall 6', has moved

inwards, thus compensating for the expected lateral spread of boron from layer 12. Next, a blanket implant of a boron dosage in the 10/13/ ion/cm/2/ range at about 55 KeV forms the P/+/ layer 16 in the field regions 9 of the substrate to complete Fig. 4. - (5) Dip etch in buffered HF to remove silicon dioxide walls 14, as shown in Fig. 5. - (6) Remove the exposed portions of layer 4 by RIE, as seen in Fig. 6. Second silicon nitride layers 8 are not wholly etched since they are twice as thick as layer 4. - (7) nip etch in buffered HF to remove silicon dioxide layer 2 and slightly undercut what remains of silicon nitride layer 4. - (8) CVD a 250 nm silicon nitride layer 18 to form the Fig. 7 structure. - (9) RIE using CF -H gas to remove flat portions of silicon nitride layer 18 and leaving vertical sidewalls in place, as shown in Fig. 8. Silicon nitride layer A will not be removed if etching time is well controlled. Thus, polysilicon blocks 6 are completely covered with silicon nitride during the oxidation that follows. - (10) Grow dry wet dry semi-recessed silicon dioxide over field regions 9 to that thickness which in conjunction with P layer 16 meets the desired thick-oxide threshold voltage for the completed ROI in Fig. 9. Silicon nitride layer 18 is in direct contact with the surface of substrate 1, thus preventing oxidation under active device regions 10 or bird's beak. - (11) Suitable dip etching or RIE are used to remove the oxide polysilicon-nitride structure covering the active device regions 10 to complete the structure shown in Fig. 10. The structure is then ready for fabrication of MOSFETs and N/+/ diffusion and polysilicon interconnections in region 10 and over the semi-recessed silicon dioxide regions 20. - This first process sequence can be modified to yield a fully recessed silicon dioxide structure. The necessary modifications are as follows. First, silicon nitride layer 8 is deposited as thick as layer 4 so that it is completely removed during step 6, and the heavy dose boron implant in step 4 is postponed. The structure is shown in Fig. 11. - Steps (7), (8) and (9) are followed without modifications. Then, before growing thick silicon dioxide as in step (10), RIE exposed the polysilicon layer 6 and the substrate. The substrate field regions can be etched deeper than the thickness of polysilicon layer 6 since silicon nitride layer 4 masks against further etching into the active device region 10, as seen in Fig. 12. - The fully-recessed silicon dioxide' structure is completed by blanket implantation of P/+/ layer 16 and thermal growth of thick silicon dioxide 20, as shown in Fig. 13. - In this second process, the spacing between the P/+/ layer 16 and device region 10 is determined by the relatively thin sidewalls 18. Larger spacings are obtained with the following third process. - (1) As in the above second process, form a stack made up of SO nm of thermal silicon dioxide layer 2; 50 nm of CVD silicon nitride layer 4; 500 nm of N polysilicon layer 6; a second silicon nitride layer 8 as thick as the first layer 4; and a top lying 50 nm layer 29 of CVD silicon dioxide. Layer 29 was not required in the first and second processes. Its purpose is to protect silicon nitride layer 8 during the first RIE etching in step (2). - (2) After defining the isolation pattern in the photoresist, RIE through the stack down to layer 4. ROI will be formed within these etched regions surrounded by active device regions 10, as shown in Fig. 14. It is important to etch this hole with near vertical sidewalls to be able to preserve the resolution of the ROI boundary after the lateral oxidation of the polysilicon layer 6 in step (4). - (3) Ion implant a light boron dose to form layer 12 which will determine the doping concentration around the ROI boundary. Dip etch in buffered HF to remove what remains of silicon dioxide layer 29, as shown in Fig. 15. - (4) Oxidize in a wet ambient or a low-temperature high-pressure oxidation chamber to form silicon dioxide walls 14 on exposed polysilicon sidewalls, as shown in Fig. 16. Since polysilicon layer 6 is sandwiched between silicon nitride layers 4 and 8, silicon dioxide 14 does not have a bird's beak. Hence, the ROI boundary offset by this oxidation can be controlled in the sub-micrometer range, a necessary attribute of the technique if it is not going to significantly reduce the active device area. - (5) RIE exposed portions of silicon nitride layer 4 and what remains of the second silicon nitride layer 8. Continue this etching to remove exposed silicon dioxide layer 2 to complete Fig. 17. This etching also reduces the height of the silicon dioxide walls 14. - (6) Using low pressure CVD, deposit silicon nitride layer 26 conforming to the profile of the structure. The thickness of this layer should be less than half the height of the step formed by layers 2, 4 and sidewall 14, but no less than 100 nm. - (7) RIE using CF(4)-H(2) gas to remove flat portions of layer 26, only leaving sidewalls 26' in place, as seen in Fig. 18. - (8) Dip etch in buffered HF to remove silicon dioxide walls 14. - (9) RIE exposed regions of the substrate and what remains of polysilicon layer 6. The depth of the trench 28 etched in the subtrate can be larger than the thickness of polysilicon layer 6 since silicon nitride layer 4 masks the substrate of active device regions 10 once polysilicon layer 6 has been consumed, as seen in Fig. 19. The opposite situation, when the trench depth is less than the polysilicon thickness, is not probable since ROI trenches are at least 250 nm, which is enough polysilicon thickness to make the size of the step mentioned in (6) high enough so that the spacer 26' formed thereon are are at least 100 nm wide. Notice that what remains of layer 12 has been determined by the silicon dioxide growth of step (4) and the silicon nitride deposition and anisotropic

etching of steps (6) and (7), both of which are well controlled processes and, likewise for the amount of boron doping remaining in 12'. In the first and second processes given in conjunction with Figs. 2-13, the polysilicon oxidation in step (4) was bypassed leaving the spacers 26' (18' in Figs. 213) solely determining the extent of 12' (compare the cross-section of Fig. 19 with that of Fig. 12). These first and second processes would be chosen when the

amount of boron needed to dope the channel stopper around the ROI perimeter is small as, for instance, for shallow trenches. - (10) Blanket implant boron to form P(+) layer 30 at the bottom of trench 28. - (11) Deepen and fill the trench 28 with thermal silicon dioxide 31 until its surface is coplanar with layer 2. This heat cycle, typically lasting between 2 and 3 hours, drives the boron in layers 12' and 30 to form merging channel stoppers around the sidewalls and bottom of the ROI structure, respectively. Moreover, the silicon nitride spacers 26' prevent the growth of bird's beak. The ROI structure is completed by dip etching in warm phosphoric acid to remove nitride layers 4 and spacers 26', as seen in Fig. 20. - A fourth process to form P(+) -channel stoppers on the sidewalls of a fully recessed oxide isolation is given wherein the process sequence is that of Figs. 14-17 up to and including step (5) thereof. - The fourth process continues at the point of Fig. 17 as follows: (1) RIE in SF(6) or SF(6) + C1(2) to form trenches in the substrate with vertical walls and remove what remains of polysilicon layer 6. Layer 4 masks the substrate thereunder after all of layer 6 is removed.

☐ 4. Document ID: NN73012567

L6: Entry 4 of 4 File: TDBD Jan 1, 1973

TDB-ACC-NO: NN73012567

DISCLOSURE TITLE: Low Temperature Photoresist Mask Etching of Silicon Nitride. January 1973.

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, January 1973, US

VOLUME NUMBER: 15
ISSUE NUMBER: 8
PAGE NUMBER: 2567

PUBLICATION-DATE: January 1, 1973 (19730101)

CROSS REFERENCE: 0018-8689-15-8-2567

DISCLOSURE TEXT:

1p. Silicon nitride may be etched under relatively mild conditions by employing an ammonium bifluoride and water solution as the etchant, and standard negative or positive photoresist material as the etchant resist. - Unless the silicon nitride has been freshly deposited, surface pretreatment is required before etching. The pretreatment comprises cleaning the surface of the silicon nitride in a strongly oxidizing medium, such as a 9:1 mixture of sulfuric and nitric acids. The cleaned surface is purged of moisture, for example, by placing in a vacuum oven for at least thirty minutes at 200 degrees C or by applying a silizane material such as HMDS, spin

drying, applying a fluorocarbon material such as FREON*, spin drying, and then baking in an oven at 160 degrees C. - Immediately after drying the cleaned surface, conventional photoresist procedures are carried out for selectively masking the silicon nitride to be etched. The masked silicon nitride is etched in a solution of ammonium bifluoride (NH(4)HF(2)) in deionized water. The formal concentration should be in the range 0.5+/- 0.05, to yield an etch rate of approximately 75 angstroms per minute at 90 degrees C. For resist materials that tend to flow at the aforementioned temperature, the temperature may be reduced to 80 degrees C with a corresponding reduction in etch rate of approximately 30 angstroms per minute. * Trademark of E. I. du Pont de Nemours & Co.

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Terms	Documents
(silicon adj nitride) same etch same fluorocarbon$	4

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